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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,264	01/29/2002	Koji Tomioka	NEC01P260-HYa	4190

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EXAMINER	
KOROBOV, VITALI A	
ART UNIT	**PAPER NUMBER**
2155	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/058,264	TOMIOKA, KOJI	
	Examiner	Art Unit	
	Vitali Korobov	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO RCE

1. This action is responsive to the amendment filed on 12/20/2006. Claim 1 was amended. New claims 21-24 were added. Accordingly, claims 1-24 are currently pending and have been examined in this Office Action.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous office action has been withdrawn pursuant to 37 CFR 1.114. The Applicant's submission filed on 12/20/2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised

of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the U. S. Patent No. 6,418,479 B1 issued to Houssein et al., hereinafter Houssein, in view of the U. S. Patent No. 6,633,916 B2, issued to Kauffman, hereinafter Kauffman.

As per claim 1, Houssein teaches a clustered computer system comprising: a plurality of CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3); and a plurality of input/output control apparatuses (2:66-3:13, claim 5, Fig. 3), wherein said CPU and memory installed apparatuses and said input/output control apparatuses are connected to each other by a network (2:22-37, 3:14-25, claim 5, Fig. 3).

Houssein does not explicitly teach a system wherein causing said CPU and memory installed apparatuses to transmit an input/output instruction to at least one of said plurality of input/output control apparatuses assigned in advance.

However, Kauffman, in analogous art, directed to communications between computer resources, and CPUs memories and I/O devices in particular, teaches a system wherein causing said CPU and memory installed apparatuses to transmit an input/output instruction to at least one of said plurality of input/output control apparatuses assigned in advance (4:46-61, where Kauffman assigns different CPU,

memory blocks and I/O devices to different logical partitions, wherein CPUs, memory, and I/O ports are assigned together into logical groups - partitions).

Therefore, it would have been obvious to one of ordinary skills in the arts at the time the invention was made to combine the teaching of Houssein with the above cited teachings of Kauffman in order to provide a computer system design which provides improved flexibility, resource availability and scalability (See Kauffman, 4:20-30). Houssein, with incorporated therein teachings of Kauffman, is hereinafter referred to as modified Houssein.

As per claim 2, modified Houssein teaches a computer system comprising: a plurality of CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3); a plurality of input/output control apparatuses (2:66-3:13, claim 5, Fig. 3), and a network connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other (2:22-37, 3:14-25, claim 5, Fig. 3), wherein each of said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by at least one CPU of said plurality of CPU and memory installed apparatuses to at least one of said input/output control apparatuses assigned in advance to said at least one CPU and memory installed apparatuses via said network, and receives a response from at lease one of said input/output control apparatuses via said network (2:22-37, 3:14-25, claim 5, Fig. 3), and wherein each of said input/output control apparatuses comprises communication means for receiving an input/output instruction from at least one CPU and memory installed apparatuses assigned in

advance to at least one of said plurality of input/output control apparatuses via said network, and transmits a response to said input/output instruction to said at least one CPU and memory installed apparatuses via said network (2:22-37, 3:14-25, claim 5, Fig. 3, and Kauffman, 4:46-61).

As per claim 3, modified Houssein teaches a computer system according to claim 2, wherein said communication means of each of said input/output control apparatuses comprises: means for receiving the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 4, modified Houssein teaches a computer system according to claim 2, wherein said communication means of each of said CPU and memory installed apparatuses comprises: means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 5, modified Houssein teaches a computer system according to claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 6, modified Houssein teaches a computer system according to claim 3, wherein said communication means of each of said CPU and memory installed apparatuses comprises: means for receiving a response as being effective only when the source of the response received via said network is an input/output control

apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 7, modified Houssein teaches a computer system according to claim 5, wherein said communication means of each of said CPU and memory installed apparatuses comprises: means for communicating with other CPU and memory installed apparatuses via said network.

As per claim 8, modified Houssein teaches a computer system according to claim 7, wherein the communications between said plurality of CPU and memory installed apparatuses are communications for accessing memories installed on other CPU and memory installed apparatuses.

As per claim 9, modified Houssein teaches a computer system according to claim 2, further comprising: means for, when either one of said CPU and memory installed apparatuses fails to operate due to a fault, assigning said input/output control apparatuses which has been used by a faulty CPU and memory installed apparatuses to another normal CPU and memory installed apparatuses hereby to continue system operation (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 10, Houssein teaches a computer system according to claim 9, wherein an active one of the CPU and memory installed apparatuses which is using another input/output control apparatuses is used as said other normal CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 1 1 , modified Houssein teaches a computer system according to claim 9, further comprising a backup CPU and memory installed apparatuses, said

backup CPU and memory installed apparatuses being used as said other normal CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 12, modified Houssein teaches a computer system according to claim 2, further comprising: at least one backup input/output control apparatuses, and means for, when either active one of said input/output control apparatuses fails to operate due to a fault, assigning said backup input/output control apparatuses to said CPU and memory installed apparatuses which has been using the faulty input/output control apparatuses thereby to continue system operation (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 13, modified Houssein teaches a computer system comprising: a CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3); an input/output control apparatuses (2:66-3:13, claim 5, Fig. 3); and a communication cable connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other (2:22-37, 3:14-25, claim 5, Fig. 3), wherein said CPU and memory installed apparatuses having communication means for transmitting an input/output instruction issued by said CPU to said input/output control apparatuses via said communication cable, and receives a response from said input/output control apparatuses via said communication cable (2:22-37, 3:14-25, claim 5, Fig. 3), and wherein said input/output control apparatuses comprising communication means for receiving an input/output instruction from said CPU and memory installed apparatuses via said communication cable, and transmits a response to said input/output instruction to said CPU and

memory installed apparatuses via said communication cable (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 14, modified Houssein teaches a CPU and memory installed apparatuses comprising: at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3); communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatuses which has been assigned in advance, and receiving a response from said input/output control apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3); and a single board on which said CPU, said memory, and said communication means are mounted (2:66-3:13, claim 5, Fig. 3).

As per claim 15, modified Houssein teaches a CPU and memory installed apparatuses according to claim 14, wherein said communication means comprises: means for receiving said response as being effective only when the source of the received response is the input/output control apparatuses which has been assigned in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 16, modified Houssein teaches an input/output control apparatuses comprising: an input/output control circuit for controlling a peripheral device based on an input/output instruction (2:66-3:13, claim 5, Fig. 3); and communication means for communicating with an external circuit comprising a CPU and memory installed apparatus, for receiving an input/output instruction from said CPU and memory installed apparatuses which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said

input/output instruction to said CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 17, modified Houssein teaches an input/output control apparatuses according to claim 16, wherein said communication means comprises: means for receiving said input/output instruction as being effective only when the source of the received input/output instruction is the CPU and memory installed apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 18, modified Houssein teaches a computer system according to claim 2, wherein each of said plurality of input/output control apparatus further comprises and input/output (I/O) device (2:66-3:13, claim 5, Fig. 3).

As per claim 19, modified Houssein teaches a computer system according to claim 18, wherein said input/output (I/O) device is connected to a peripheral device (Fig. 3).

As per claim 20, modified Houssein teaches a computer system according to claim 18, wherein said input/output (I/O) device is connected to a second network (Fig. 3).

As per claim 21, modified Houssein teaches the clustered computer system according to claim 1, wherein when one of said plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, an other one of said plurality of CPU and memory installed apparatuses begins operation with said one of said plurality of input/output control apparatuses (Kauffman, 8:10-16).

As per claim 22, modified Houssein teaches the computer system according to claim 2, wherein said communication means comprises a plurality of ports (Kauffman, 4:46-61).

As per claim 23, modified Houssein teaches the computer system according to claim 22, wherein each of said plurality of input/output control apparatuses is allocated to at least one of said plurality of ports of said communication means (Kauffman, 8:1-9 - partition has full ownership and control of hardware components, such as ports, assigned to it and only the partition itself may release its components).

As per claim 24, modified Houssein teaches the computer system according to claim 22, wherein when one of the plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, said one of said plurality of input/output control apparatuses is newly allocated to any one of the plurality of ports to which said one of said plurality of input/output control apparatuses was not previously allocated (Kauffman, 8:10-16 - reassignment of hardware resources).

5. **Examiner's note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Response to Arguments

6. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection, necessitated by the Applicant's amendment.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objection made. Applicant must show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vitali Korobov whose telephone number is 571-272-7506. The examiner can normally be reached on Mon-Friday 8a.m. - 4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on (571)272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Vitali Korobov
Examiner
Art Unit 2155

03/04/2007
VAK

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SUPERVISORY PATENT EXAMINER